

IN THE CLAIMS:

1. (Currently Amended) A method for manufacturing a semiconductor device, comprising:

forming a gate structure over a substrate, said gate structure including a gate dielectric, a polysilicon gate electrode located over said gate dielectric, and a protective layer located over said polysilicon gate electrode over a substrate;

forming source/drain regions in said substrate proximate said polysilicon-gate electrode gate structure;

forming a first silicidation metal in contact with said source/drain regions, said protective layer separating said polysilicon gate electrode from said first silicidation metal;

forming a blocking layer over said source/drain regions in a step from said first silicidation metal, said blocking layer comprising a metal silicide;

removing said protective layer from over said polysilicon gate electrode after forming said blocking layer;

forming a second silicidation metal in contact with said polysilicon gate electrode and in contact with said blocking layer; and

siliciding said polysilicon gate electrode using said second silicidation metal to form a silicided gate electrode in a later step, said blocking layer protecting said source/drain regions from said siliciding.

Claim 2 (Canceled)

3. (Original) The method as recited in Claim 1 wherein said blocking layer is a silicided source/drain contact region.

4. (Original) The method as recited in Claim 1 wherein said silicided gate electrode comprises a different metal silicide than said blocking layer.

5. (Original) The method as recited in Claim 4 wherein said blocking layer comprises a cobalt silicide and said silicided gate electrode comprises a nickel silicide.

6. (Original) The method as recited in Claim 1 wherein said blocking layer has a thickness ranging from about 10 nm to about 35 nm.

Claim 7 (Canceled)

8. (Currently Amended) The method as recited in ~~Claim 7~~Claim 1 wherein said protective layer is a silicon nitride protective layer.

9. (Original) The method as recited in Claim 1 wherein siliciding said polysilicon gate electrode to form a silicided gate electrode includes fully siliciding said polysilicon gate electrode to form a fully silicided gate electrode.

10. (Currently Amended) A method for manufacturing an integrated circuit, comprising:

forming semiconductor devices over a substrate, including;

forming a gate structure over a substrate, said gate structure including a gate dielectric, a polysilicon gate electrode located over said gate dielectric, and a protective layer located over said polysilicon gate electrode~~over a substrate~~;

forming source/drain regions in said substrate proximate said polysilicon gate electrode structure;

forming a first silicidation metal in contact with said source/drain regions, said protective layer separating said polysilicon gate electrode from said first silicidation metal;

forming a blocking layer over said source/drain regions from said first silicidation metal in a step, said blocking layer comprising a metal silicide;

removing said protective layer from over said polysilicon gate electrode after forming said blocking layer;

forming a second silicidation metal in contact with said polysilicon gate electrode and in contact with said blocking layer; and

siliciding said polysilicon gate electrode using said second silicidation metal to form a silicided gate electrode ~~in a later step~~, said blocking layer protecting said source/drain regions from said siliciding; and

forming interconnects within dielectric layers located over said substrate for electrically contacting said semiconductor devices.

Claim 11 (Canceled)

12. (Original) The method as recited in Claim 10 wherein said blocking layer is a silicided source/drain contact region.

13. (Original) The method as recited in Claim 10 wherein said silicided gate electrode comprises a different metal silicide than said blocking layer.

14. (Original) The method as recited in Claim 13 wherein said blocking layer comprises a cobalt silicide and said silicided gate electrode comprises a nickel silicide.

15. (Original) The method as recited in Claim 10 wherein said blocking layer has a thickness ranging from about 10 nm to about 35 nm.

Claim 16 (Canceled)

17. (Currently Amended) The method as recited in ~~Claim 16~~Claim 10 wherein said protective layer is a silicon nitride protective layer.

18. (Original) The method as recited in Claim 10 wherein siliciding said polysilicon gate electrode to form a silicided gate electrode includes fully siliciding said polysilicon gate electrode to form a fully silicided gate electrode.

19. (Previously Presented) The method as recited in Claim 1 wherein siliciding said polysilicon gate electrode to form said silicided gate electrode occurs prior to siliciding any portion of the polysilicon gate electrode.

20. (Previously Presented) The method as recited in Claim 10 wherein siliciding said polysilicon gate electrode to form said silicided gate electrode occurs prior to siliciding any portion of the polysilicon gate electrode.